EXHIBIT 3

UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF MASSACHUSETTS

SINGULAR COMPUTING LLC, Plaintiff, v. GOOGLE LLC, Defendant.	Civil Action No. 1:19-cv-12551-FDS Hon. F. Dennis Saylor IV

OPENING EXPERT REPORT OF DR. JOHN L. GUSTAFSON REGARDING THE INVALIDITY OF THE ASSERTED PATENTS

[redacted]

Executed on December 22, 2022 in Glendale, Arizona.

DocuSigned by:
Dr. John L Gustafson
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John L. Gustafson, Ph.D.

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I. INTRODUCTION

1. My name is John Gustafson, and I have been retained by counsel for Defendant Google LLC ("Google") in this case to analyze and opine on the validity of U.S. Patent Nos. 9,218,156 ("the '156 patent") and 8,407,273 ("the '273 patent") (the "asserted patents"), asserted in this matter by Plaintiff Singular Computing LLC, and certain related issues, as noted below.

2. I am being compensated for my work in this matter at my standard rate of $250.00 per hour and am being reimbursed for any expenses incurred in relation to my work on this matter. My compensation is not contingent upon the outcome of this matter or the substance of my testimony.

3. I expect to be called to provide expert testimony regarding opinions formed as a result of my analysis of the issues considered in this Report if asked to do so by the Court or counsel for Google. If asked to do so, I may also provide testimony describing the state of the art before and during the time of the alleged invention.

4. In reaching the conclusions described herein, I have considered the documents and materials identified in **Exhibit A**. My opinions are also based on my education, training, research, knowledge, and personal and professional experience.

5. I reserve the right to modify or supplement my opinions, as well as the basis for my opinions, in light of any documents, testimony, expert opinions, or other evidence or information that may emerge during the course of this litigation, including any depositions that have yet to be taken.

6. I understand that Plaintiff may submit an expert report responding to this Report. I reserve the right to rebut any opinions in that report or any other issues asserted by Plaintiff.

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II. SCOPE OF ASSIGNMENT AND SUMMARY OF OPINIONS

A. Claims Analyzed

7. I understand that Plaintiff asserts claim 7 of the '156 patent and claim 53 of the '273 patent (the "asserted claims").

B. Issues Considered

8. I was asked to provide my opinions on the validity of the asserted claims of the '156 and '273 patents. Specifically, I was asked to provide my opinions on the following: whether the asserted claims are anticipated by the prior art, whether the asserted claims would have been obvious over the prior art, to what the asserted claims are directed, and whether the asserted claims embody a concrete technological innovation.

9. I was given access to all materials I felt were necessary to render these opinions.[1]

C. Summary of Opinions

1. The Asserted Claims are Anticipated by the Prior Art

10. It is my opinion that the asserted claims of the '156 and '273 patents are invalid as anticipated in light of the prior art, for at least the reasons set forth in this Report.

2. The Asserted Claims Would Have Been Obvious Over the Prior Art

11. It is my opinion that the asserted claims of the '156 and '273 patents are invalid as rendered obvious in light of the prior art, for at least the reasons set forth in this Report.

[1] Unless otherwise indicated in this Report, I have added emphases to quotations, and omitted any internal quotation marks, brackets, cites, ellipses, and footnotes from them.

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3. The Asserted Claims are Directed to Performing Less Precise Mathematical Calculations to Achieve Results that Differ From the Exact Mathematical Results

12. It is my opinion a person of ordinary skill in the art would have found that the asserted claims of the '156 and '273 patents are directed to performing less precise mathematical calculations to achieve results that differ from the exact mathematical results, for at least the reasons set forth in this Report.

4. The Asserted Claims Do Not Embody a Concrete Technological Solution

13. It is my opinion that, for at least the reasons set forth in this Report, for each of the asserted claims of the '156 and '273 patents, none of the limitations embody a concrete technological solution, and considering the limitations as a combination adds nothing that is not already present when the limitations are considered individually.

D. Materials Considered

14. As part of my preparation for writing this Report, I have reviewed and considered the materials identified in **Exhibit A** to this Report.

15. In addition to the documentary evidence I considered, I also relied in part upon discussions with individuals with pertinent knowledge, and have endeavored to note in this Report where my opinions rely in part on such discussions. For example, I met with Dr. Miriam Leeser on the following dates in 2022: November 17; December 1; December 13; and December 14.

16. Below I provide the details of my analysis, and the conclusions that form the basis of any testimony that I give below. Such testimony may include appropriate visual aids, some or all of the data or other documents and information cited herein or identified in **Exhibit A**, and additional data or other information identified in discovery, to support or summarize my

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opinions. For example, I may include information cited by Plaintiff's expert(s) as well as witness testimony.

III. QUALIFICATIONS AND EXPERIENCE

17. I have over forty years of experience in the computer science field. My focus has been on computer arithmetic (*i.e.*, the ways that computing devices perform mathematical operations) and parallel processing (*i.e.*, techniques to accelerate computing tasks by breaking them down into smaller tasks that are simultaneously executed), topics that are explored in greater detail in Section V below.

18. I am a Visiting Scholar at Arizona State University in Tempe, Arizona, collaborating with faculty and students on high-performance and quantum computing research. Previously, between August 2015 – November 2021, I was Professor in the School of Computing, National University of Singapore.

19. In 1977, I earned my B.S. in Applied Mathematics, with honors, from the California Institute of Technology. Algorithms I had developed for solving systems of equations on Hewlett-Packard computing devices were published while I was still an undergraduate.

20. In 1981 and 1982, I earned my M.S. and Ph.D., respectively, in Applied Mathematics from Iowa State University. Since completing my doctoral degree, I have held numerous positions—in academia, the private sector, and at U.S. federal research institutions—as a professor, engineer, and scientist in the field of computer science.

21. I have published over 100 academic papers in peer-reviewed journals or textbooks. As of December 19, 2022, my published works have been cited 5,951 times (*see* https://scholar.google.com/citations?user=oqjpW64AAAAJ&hl=en).

22. In 1988, I was awarded the inaugural Gordon Bell Prize—sometimes called the "Nobel Prize of Supercomputing"—for my work that achieved thousand-fold speedups in the

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completion of computing tasks, and my creation of a novel theoretical model explaining how that was possible. The model is now called "Gustafson's law" and is taught in undergraduate and graduate-level computer science classes.

23. While leading a supercomputer project at Sun Microsystems, I patented a method of analyzing floating-point error by attaching numerical records to every datum (*Method and Apparatus for Accuracy-Aware Analysis*), which issued as U.S. Patent No. 7,448,026. I am a named inventor of a number of other issued U.S. patents.

24. Attached as **Exhibit B** is a copy of my curriculum vitae.

IV. UNDERSTANDING OF PATENT LAW AND LEGAL STANDARDS

25. I have been informed by counsel for Google of the relevant legal standards that apply in evaluating the validity of a patent. I am not an attorney and am relying on instructions from Google's attorneys for these legal standards. Below I describe my understanding of these legal standards.

A. Burden of Proof Regarding Patent Invalidity

26. I understand that patents are presumed valid and that invalidity must be shown by "clear and convincing" evidence. I understand that the "clear and convincing" evidence standard is higher than a preponderance of the evidence but lower than beyond a reasonable doubt, and that clear and convincing evidence is evidence that produces an abiding conviction that the truth of a fact is highly probable.

B. Patent Eligibility

27. I understand the patent laws limit the subject matter that is eligible for patent protection and that one may not obtain a patent on an abstract idea. I have not been asked to offer an opinion whether the asserted patent claims are patent eligible, but I have been asked to offer opinions regarding two sub-issues that I understand may be relevant to this issue.

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28. I have been asked to offer an opinion about what the asserted claims are directed to. I understand that in determining what the claims are directed to, the claims are considered in their entirety to ascertain their character as a whole. I understand that while the specification may be useful to illuminate what the claims are directed to, any reliance on the specification must always yield to the claim language. I understand that one question that may be considered in this context is whether the claims are directed to an improvement in computer functionality, including whether they purport to improve the functioning of the computer itself, or instead are whether the focus of the claims is on a process for which computers are invoked merely as a tool.

29. I have been asked to offer an opinion whether the asserted claims embody a concrete technological innovation. I understand, for example, that a solution that is described and claimed generically is not a concrete technological innovation.

C. Anticipation

30. I understand that a patent claim is "anticipated" if each and every element of the claim, as properly construed, has been disclosed in a single prior art reference either expressly or inherently (i.e., necessarily present even if not expressly stated), and the claimed arrangement or combination of those elements has been disclosed, either expressly or inherently, in the same prior art reference. I also understand that there are various ways that to show that a patent claim is anticipated, such as:

i) if the claimed invention was already publicly known or publicly used by others in the United States before the priority date;

ii) if the claimed invention was already being used in the United States before the priority date and that use was not primarily an experimental use (a) controlled by the inventor, and (b) to test whether the invention worked for its intended purpose; and

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H. Hardware for Implementing Mixed- and Low-Precision Systems

187. It is well-known that low-precision systems and mixed-precision systems, *i.e.*, systems that can perform lower-precision and higher-precision operations, can be implemented on various types of hardware. Below, I discuss some examples.

1. Field-Programmable Gate Arrays ("FPGAs")

188. A field-programmable gate array ("FPGA") is "a configurable integrated circuit," Patterson at G-6, without a fixed function at the time of its manufacture. An FPGA is comprised of "large numbers of programmable logic elements on a single chip. "The speed and size of those circuits improve at the same rate as [traditional] microprocessors' size and speed, since they rely on the same technology." Cloutier at 1:28–31. The programmability of an FPGA being referenced is not merely limited to *software* executing on FPGA hardware, but rather, to aspects of the hardware itself. This enables users to define the structure of application-specific hardware computation units that can later be completely redesigned through "programming" the FPGA.[17] Users can configure FPGAs to perform the fundamental logic operations for user-defined arithmetic.

189. In other words, FPGAs provide custom hardware that is adaptable for application-specific computation design. *See* Sahin at 445. Changes to the design of an FPGA can be made simply by reprogramming it, and thus, changes can be accomplished within a few hours, resulting in significant cost and time savings. *See* Sahin at 445.

[17] *See, e.g.*, Shirazi at 23790 ("Eighteen and sixteen bit floating point adders/subtracters, multipliers, and dividers have been synthesized for Xilinx 4010 FPGAs."); Shirazi at 23796 ("To implement single precision floating point arithmetic units . . . the size of floating point arithmetic units would increase between 2 to 4 times over the 18 bit format. A multiply unit would require two Xilinx 4010 chips . . . .").

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190. Since at least as early as 1995, FPGAs have been capable of implementing floating-point arithmetic. For example, in 1995, Shirazi wrote that "[u]ntil recently, any meaningful floating point arithmetic has been virtually impossible to implement on FPGA based systems due to the limited [transistor] density and speed of older FPGAs." Shirazi at 23790. Shirazi successfully synthesized "[e]ighteen and sixteen bit floating point adders/subtracters, multipliers, and dividers . . . for Xilinx 4010 FPGAs." Shirazi at 23790; *see also* Aty at 274 ("Recently, the density and speed of FPGA are increased, so it's easy to implement floating-point arithmetic on it."); Sahin at 445-46 ("Several researchers [LMMSU98, LJC96] have implemented floating point adders and multipliers on FPGAs, which meet IEEE 754 floating point format. Most commercial floating point implementations provide units that comply with the IEEE 754 standard [Nall01].").

191. FPGAs are particularly well suited for parallelization because they can implement systolic parallelism, creating an assembly line of functional units that does not need to reference main memory except for the initial data and the final result.

2. Application-Specific Integrated Circuits ("ASICs")

192. ASICs are circuits used for special-purpose computers that are built to solve specific problems. ASICs allow for the arrangement of arithmetic units to optimize for the computation pattern of a particular problem. For instance, GRAPE-3 is an example of an implementation of ASICs, in which a mathematical equation for the gravitational interaction force is calculated in a massively parallel manner.

193. CNAPS also operates using ASICs, on Very Large Scale Integration ("VLSI") silicon chips that are optimized for the specific artificial neural network computations that the CNAPS System is designed to perform. Hammerstrom-1995 at 335; Kinser at 25655 ("The

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[CNAPS Sequencer] ASIC chip controls the operation of the [processing node] array as well as broadcasting data over the input bus and reading the results from the output bus.").

194. Because ASICs can be customized to solve a particular problem, they allow users to optimize the chip architecture in view of the computational characteristics of a problem, providing for a high functional density, meaning that the amount of necessary silicon per operation is minimized. Hammerstrom-1995 at 336. In other words, ASICs can make more operations possible per-second at a lower cost. Hammerstrom-1995 at 336.

195. ASICs lack, however, the flexibility to be reprogrammed or rearranged as FPGAs can be.

3. Central Processing Units ("CPUs")

196. CPUs, also called "processors," are "[t]he active part of a computer, which contains the datapath and control and which adds numbers, test numbers, signals I/O devices to activate, and so on." Patterson at 20.

197. CPUs consist of silicon transistors that execute instructions or programs, including performing arithmetic and logic operations.

198. CPUs are often connected to other components of a computing device, including memory or interfaces.

199. In addition to performing higher precision operations, CPUs can also be programmed to perform lower precision arithmetic operations. *See, e.g.*, Tong at 278 ("To determine the impact of different mantissa and exponent bitwidths, we emulated in software different bitwidth FP units by replacing each FP operation with a corresponding function call to our FP software emulation package that initially implements the IEEE-754 standard (Fig. 5). Careful modifications to the FP emulation package allowed us to emulate different mantissa and

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exponent bitwidths. Then, each program was run using the modified FP package, and the results were compared to determine application accuracy.").

4. Graphics Processing Units ("GPUs")

200. GPUs are specialized processors "optimized for 2D and 3D graphics, video, visual computing, and display." Patterson 2012 at A-3.

201. GPUs have long been known in the art. For example, the first GPU from NVIDIA was the GeForce 256, which was introduced in 1999. Lindholm at 39. The GeForce 256 contained "a fixed-function 32-bit floating-point vertex transform and lighting processor and fixed-integer pixel-fragment pipeline, which were programmed with OpenGL and the Microsoft DX7 API." Lindholm at 39. A later NVIDIA model, the GeForce 8800, released in 2006, included "texture unit[s]" that supported "high-dynamic-range (HDR) 16-bit and 32-bit floating-point data format filtering." Lindholm at 39, 47.

I. Mixed-Precision Systems

202. Mixed-precision systems are those systems that employ both lower-precision and higher-precision processing capabilities. Mixed-precision systems are well-known in the art.

203. The GeForce 8800 GPU from NVIDIA is one example of mixed-precision processors because it supported "high-dynamic-range (HDR) 16-bit and 32-bit floating-point data format filtering." Lindholm at 39, 47.

204. As I explain below in more detail, the VFLOAT system, the CNAPS system, and the GRAPE-3 system are also examples of mixed-precision systems.

VI. OVERVIEW OF THE ASSERTED PATENTS

A. The '156 Patent

205. The '156 patent is titled "Processing with Compact Arithmetic Processing Element" and is directed to "[a] processor or other device, such as a programmable and/or

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VII. CLAIM CONSTRUCTION

210. I have been instructed and understand that claim construction is a matter of law for the Court to decide. I further understand that the Court issued a Memorandum and Order on Claim Construction ("CC Order") on July 27, 2022, setting forth the construction of various claim terms in the asserted patents. I have reviewed the Claim Construction Order, familiarized myself with the Court's construction of the relevant claim terms, and have applied the Court's rulings in reaching my opinions as set forth in this Report.

211. Specifically, I understand that the Court construed the terms "low precision and high dynamic range," "execution unit," and "first input signal representing a numerical value." More specifically, I understand that the Court construed "low precision and high dynamic range" as defined elsewhere in the claim language itself.[18] I also understand that the Court construed "execution unit" to mean "processing element comprising an arithmetic circuit paired with a memory circuit."[19]

212. I further understand that the Court construed "first input signal representing a numerical value" according to its plain and ordinary meaning.[20] The Court wrote: "Google construes the claim language such that the LPHDR execution unit operates on numerical values, which are represented by electrical signals, whereas Singular interprets the claim language such that the LPHDR execution unit operates on signals that represent numerical values. In this context, at least, that appears to be a distinction without a meaningful difference."[21] As a result, I understand that the Court held: "[T]he distinction between a signal (which represents an abstract

[18] CC Order at 16–17.
[19] CC Order at 25.
[20] CC Order at 30.
[21] CC Order at 27–28.

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value) and a value (which exists in the physical form of an electrical signal) is meaningless in this context . . . ."[22]

213. I further understand that the Court addressed the parties' dispute over whether the claim term "repeated execution" was indefinite, reaching the conclusion that it did not find that this term was indefinite.[23]

214. For claim terms not submitted for construction, or for claim terms where I am otherwise applying their "plain meaning," I have given claim terms their ordinary and customary meaning within the context of the patent in which the terms are used, *i.e.*, the meaning that the term would have had to a person of ordinary skill in the art in question at the time of the alleged invention in light of the intrinsic evidence, including the language of the claim itself and of other issued claims, the patent specification, and the prosecution history.

VIII. INVALIDITY OVER PRIOR ART

215. For the reasons I explain in Subsections VIII.A–K below, it is my opinion that the asserted claims are anticipated by or rendered obvious by various prior art systems.

A. Work By Dr. Miriam Leeser on the VFLOAT Library

216. As I explain below, it is my opinion that the claims are anticipated or rendered obvious by a system made, used, and disclosed by Dr. Miriam Leeser of Northeastern University in Boston, MA. I refer to this system in this Report as the "VFLOAT System."

217. Below I provide a description of the VFLOAT System and its components. My understanding of the facts recited below is based on my conversations with Dr. Leeser on November 17, 2022, December 1, 2022, December 13, 2022, and December 14, 2022, and is confirmed by my review of the Report of Dr. Miriam Leeser ("Leeser-Report").

[22] CC Order at 30.
[23] CC Order at 15–16.

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to performing less precise mathematical calculations to achieve results that differ from the exact mathematical results.

XI. THE ASSERTED CLAIMS DO NOT EMBODY A CONCRETE TECHNOLOGICAL INNOVATION

703. In my opinion, the specific limitations of the claims, whether considered alone or in combination, do not embody a concrete technological innovation.

704. ***High dynamic range.*** The asserted claims recite specific numbers such as 1/1,000,000, or 5%, but do so using the qualifier "at least." This means that the claims recite broad, open-ended ranges, rather than embodying specific solutions. Moreover, the patents do not disclose a concrete technological innovation that arises from the particular numbers recited.

705. The asserted claims each require that the dynamic range of possible inputs is *at least* as wide as from 1/1,000,000 to 1,000,000. The well-known IEEE-754 standard, which uses an 8-bit exponent with a bias of 127, can encode numbers that are far smaller in magnitude than 1/1,000,000 and far larger in magnitude 1,000,000, allowing for inputs with a dynamic range that is at least as wide as from 1/1,000,000 to 1,000,000. This dynamic range results from the application of well-understood, routine, conventional mathematical principles to the bitwidth of the exponent and the bias that is used.

706. Because the dynamic range recited in the asserted claims uses the qualifier "at least," it is a broad, open-ended range rather than an embodiment of a concrete technological innovation. Indeed, as just noted, this broad, open-ended range includes the dynamic range used by the conventional IEEE-754. In my opinion, the fact that the dynamic range used by IEEE-754 satisfies the limitation confirms that it does not disclose a concrete technological innovation.

707. The patent does not disclose a concrete technological innovation arising from using a dynamic range of *at least* as wide as from 1/1,000,000 to 1,000,000. Instead, the patent

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states that "implementations may vary in the dynamic range of the space of values they process," and that while this range could be from "approximately from one millionth to one million," it could also be "approximately from one billionth to one billion," or "approximately from one sixty five thousandth to sixty five thousand," or even "from any specific value between zero and one sixty five thousandth up to any specific value greater than sixty five thousand" or "in spaces with dynamic ranges that may combine and may fall between the prior examples, for example ranging from approximately one billionth to ten million." '273 Patent at 27:5–28; '156 Patent at 26:61–27:17. In my opinion, no concrete technological innovation arises from specifying that the execution unit should have a dynamic range of *at least* as wide as from 1/1,000,000 to 1,000,000.

708. ***Low precision.*** The asserted claims each require that for *at least* X=5% of the possible valid inputs, the output differs by *at least* Y=0.05% from the result of an exact mathematical calculation. In my opinion, this requirement does not embody a concrete technological innovation. The notion that, for some inputs, the output of an operation could differ by some amount from an exact mathematical calculation was well-known in the art. Indeed, in conventional binary floating-point mathematics, some amount of difference from an exact mathematical calculation for some inputs can result from conventional techniques and limitations such as such as rounding or truncating the output of an operation to correspond to the precision of the input.

709. Because both the frequency and difference required by the asserted claims are stated using the qualifier "at least," they both also are broad, open-ended ranges rather than a concrete technological innovation.

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710. Moreover, because there is no *upper* bound either on the frequency or the difference, the claims encompass even an execution unit that, for every or nearly single valid input, has outputs that differ from the exact mathematical calculation by 100% or even more.

711. For example, an execution unit that outputs 0 for any pair of non-zero multiplicands, and that outputs 1 if one of the two multiplicands is zero, would be wrong for every single valid input, and it would be hard to imagine a situation in which such an execution unit would serve any purpose—yet it falls within the broad, open-ended ranges recited in the asserted claims.

712. Likewise, an execution that randomly chooses, with equal likelihood, between 1, 2 and 3 as the output for any input pair of multiplicands would also fall within the claim scope. No matter what the input, the statistical mean of the output, over repeated execution, would be 2. For the vast majority of valid inputs, 2 would differ from the exact mathematical result by a large percentage. Such an execution unit for the multiply operation would be nonsensical, yet again it falls within the broad, open-ended ranges recited in the asserted claims.

713. In my opinion, the fact that the claims offer no guidance about how to select an acceptable *upper* limit for the frequency or the difference confirms that this limitation does not embody a concrete technological innovation.

714. The patents do not disclose a concrete technological innovation arising from having outputs that differ by at least a certain amount from an exact mathematical result at least X=5% of the time. Instead, the patent discloses that "[t]he frequency with which LPHDR arithmetic elements may yield only approximations to correct results may vary from implementation to implementation." '273 Patent at 27:29–31; '156 Patent at 27:18–20. The patent discloses that the frequency could be 1%, 2%, 5%, 10%, 20%, or 50%, and that those

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frequencies are "merely examples." '273 Patent at 27:29–62; '156 Patent at 27:18–51. The fact that even such a wide range of different frequencies are merely exemplary illustrates that choosing X=5% as the lower bound for the claimed frequency, as in the asserted claims, is not a concrete technological innovation. In my opinion, no concrete technological innovation arises from having outputs that differ by at least a certain amount from an exact mathematical result at least X=5% of the time.

715. The patents do not disclose a concrete technological innovation arising from having outputs that differ by at least Y=0.05% from an exact mathematical result. Instead, the patent discloses that "[t]he degree of precision of a 'low precision, high dynamic range' arithmetic element may vary from implementation to implementation," and could be 0.1%, 0.2%, 0.5%, 1%, 2%, 5%, 10% or 20%. '273 Patent at 26:50–27:4; '156 Patent at 26:39–60. In my opinion, no concrete technological innovation arises from having outputs that differ by at least Y=0.05% from an exact mathematical result.

716. Moreover, the asserted claims focus on the *result*—the frequency and degree of error—rather than on a technological approach used to achieve that result. This focus again confirms my opinion that the asserted claims do not embody a concrete technological innovation.

717. ***LPHDR versus traditional execution units.*** The asserted claims each require that the number of LPHDR execution units exceed by at least one hundred the non-negative integer number of execution units that are adapted to execute multiplication on floating point numbers that are at least 32 bits wide. This approach of mixing different precision execution units was well-known in the art, as I have already discussed. *See* Subsection V.H. Notably, the claim cites no concrete details regarding the configuration of the LPHDR execution units required by the claims.

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718. Because the limitation uses the qualifier "at least," it is a broad, open-ended range rather than embodying a concrete technological innovation. The claim language would encompass, for example, a device with 150 LPHDR execution units and 10 traditional execution units, but also a device with 65,536 LPHDR execution units and no traditional execution units at all, or one with 101,000 LPHDR execution units and 100,000 traditional execution units. In the first example, there would be 15 times as many LPHDR execution units as traditional execution units. In the second, there would be *only* LPHDR execution units. In the third, there would be only 1% more LPHDR execution units as there are traditional execution units. These examples reflect very different technological approaches, yet all fall within the claim scope. In my opinion, this confirms that the claims do not embody a concrete technological innovation.

719. The patent does not disclose a concrete technological innovation arising from having at least one hundred more LPHDR execution units than execution units adapted to perform multiplication on 32-bit floating point numbers. Instead, the patent discloses that the number of LPHDR execution units exceeds the number of execution units adapted to perform 32-bit floating point multiplication by "some function," noting that "[a]ny of a variety of functions may be used," including "twenty plus three times," "fifty more than five times," "one hundred more than five times," "one thousand more than five times," or "five thousand more than five times." '273 Patent at 28:3–31; '156 Patent at 25:59–28:21. In my opinion, this confirms that the one hundred LPHDR execution unit end point of the open-ended range is itself arbitrary, rather than embodying a concrete technological innovation. In my opinion, no concrete technological innovation arises from having at least one hundred more LPHDR execution units than execution units adapted to perform multiplication on 32-bit floating point numbers.

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720. ***Asserted claims as a whole.*** I have also considered the combination of the foregoing limitations, including in combination with the other limitations of the asserted claims, taking into account the claim construction order. In my opinion, considering the limitations as a combination adds nothing that is not already present when the limitations are considered individually. Indeed, because each of the limitations discussed above claims a broad, open-ended range, combining them likewise claims a broad, open-ended scope of devices, rather than embodying a concrete technological innovation.

XII. CONCLUSION

721. Based on my knowledge, experience, education, and professional judgment, my understanding of the legal standards in this case, and my review of the evidence, it is my opinion that the prior art shows that asserted claim 7 of the ’156 patent and claim 53 of the ’273 patent are invalid as anticipated and/or obvious. Furthermore, it is also my opinion that Singular cannot demonstrate any objective indicia of nonobviousness. In addition, it is also my opinion that a skilled artisan would have understood that the asserted claims are directed to performing less precise mathematical calculations to achieve results that differ from the exact mathematical results, and that the specific limitations of the asserted claims—whether considered alone or in combination—do not embody a concrete technological innovation